Ultrashort Channel Length Black Phosphorus Field-Effect Transistors

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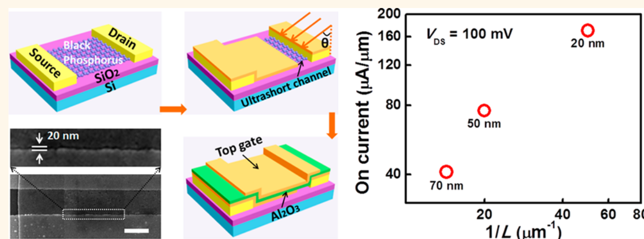
ABSTRACT This paper reports high-performance top-gated black phosphorus (BP) field-effect transistors with channel lengths down to 20 nm fabricated using a facile angle evaporation process. By controlling the evaporation angle, the channel length of the transistors can be reproducibly controlled to be anywhere between 20 and 70 nm. The as-fabricated 20 nm top-gated BP transistors exhibit respectable on-state current (174 μA/μm) and transconductance (70 μS/μm) at a V_{DS} of 0.1 V. Due to the use of two-dimensional BP as the channel material, the transistors exhibit relatively small short channel effects, preserving a decent on–off current ratio of 10^2 even at an extremely small channel length of 20 nm. Additionally, unlike the unencapsulated BP devices, which are known to be chemically unstable in ambient conditions, the top-gated BP transistors passivated by the Al_2O_3 gate dielectric layer remain stable without noticeable degradation in device performance after being stored in ambient conditions for more than 1 week. This work demonstrates the great promise of atomically thin BP for applications in ultimately scaled transistors.



KEYWORDS: black phosphorus · 2D semiconductors · field-effect transistors · device scaling · ultrashort channel length

As the scaling of the silicon-based transistor approaches its physical limit, exploratory research is needed to develop alternative channel materials for future sub-5 nm gate length devices. For such an ultrascaled electronic device, short channel effects would severely limit its performance and operation.[1] In order to suppress the short channel effects at extreme scaling limits, the thickness of the channel material needs to be less than roughly one-third of the gate length in order to allow the gate to retain its effective electrostatic control of channel carrier concentration.[2,3] However, for conventional semiconductors, the rough surface of the ultrathin body (a few atomic layers) would lead to severe surface scattering for carriers, resulting in severely degraded carrier mobility.[4,5] In this regard, two-dimensional (2D) layered semiconductors are excellent candidates for future ultimately scaled electronic devices because they are atomically smooth and free of dangling bonds/defect states, which lead to intrinsically low surface scattering.[6] Another important advantage of these atomically thin 2D semiconductors is their immunity to short channel effects due to their small thickness.[7] Current research in 2D layered materials primarily focuses on graphene,[8−12] insulating hexagonal boron nitride,[13] and transition metal dichalcogenides (TMDCs),[14] such as tungsten diselenide (WSe_2)[4,15] and molybdenum disulfide (MoS_2).[6,7,16−22] As the most extensively studied 2D layered material, graphene possesses superior carrier mobility up to 10^5 cm^2 V^{-1} s^{-1}, but the zero band gap nature poses limitations on its applications in electronic or optoelectronic devices as graphene transistors have a very small amount of gate modulation.[23] Transistors made from monolayer or few-layer TMDCs, such as MoS_2 and WSe_2, exhibit decent on/off current ratios due to their decent band gap size and excellent current saturation characteristics.[24] However, the carrier mobility in TMDCs is much lower than that in graphene and varies largely from 10 to 200 cm^2 V^{-1} s^{-1}.[6,7] Recently, a novel elemental 2D material was isolated by mechanical exfoliation of black phosphorus (BP) crystals, an allotrope of the element phosphorus with layered structure.[25−36] Unlike semimetallic graphene, BP is a direct band gap semiconductor with a thickness-dependent band gap ranging from ∼0.3 eV (bulk) to ∼2.0 eV (monolayer).[37,38] Few-layer BP nanoflakes have been used as channel materials in field-effect transistors

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(FETs). Such BP FETs exhibit high on/off current ratios of 10^4-10^5 and room temperature field-effect mobility up to 1000 $cm^2\ V^{-1}\ s^{-1}$.[37,39,40] These desirable properties make 2D layered BP a promising candidate for high-performance electronic and optoelectronic devices, such as radio frequency transistors,[41] photodetectors,[42−46] memory devices,[47] and digital inverters.[48]

To the best of our knowledge, the smallest BP transistor demonstrated so far has a channel length of approximately 100 nm fabricated by electron beam lithography (EBL).[49] It gets significantly more challenging to further scale down the channel length to below 100 nm due to the limitations in the EBL process, e-beam resist, and lift-off process used. In this paper, we report a novel and facile process combining EBL and angle deposition[50] to fabricate top-gated BP transistors with channel lengths down to 20 nm. With the high-quality few-layer BP obtained from mechanical exfoliation and ultrashort channel length, such devices exhibit respectable on-current and transconductance up to 174 μA/μm and 70 μS/μm, respectively, at a small drain-to-source voltage of 100 mV. Additionally, although a certain amount of short channel effects are observed at a channel length of 20 nm, the transistors still manage to retain a decent on/off ratio of $\sim 10^2$, which is expected with the use of ultrathin 2D semiconductor channel material. The results demonstrate the potential of few-layer BP for ultimately scaled transistors.

RESULTS AND DISCUSSION

The fabrication process used to obtain the ultrashort channel length BP FETs is illustrated in Figure 1a. More details can be found in the Methods section. Briefly, few-layer BP nanoflakes (<10 nm) were mechanically exfoliated from bulk BP crystals and transferred onto a silicon wafer with 300 nm thick SiO_2. "Long" channel ($L \approx 1\ \mu$m) BP FETs with 50 nm thick gold (Au) source/drain (S/D) contacts were then fabricated by EBL patterning, metal evaporation, and lift-off processes (Figure 1a(i), b(i)). A second EBL step was carried out to open a window across the channel region of these "long" channel BP transistors, followed by deposition of 20 nm thick Au film intentionally evaporated with an angle (Figure 1a(ii), b(ii)). With the sample placed at an angle (θ) to the metal evaporation direction, the existing 50 nm thick Au electrodes leave a shadow behind for the second metal deposition, allowing ultrasmall gaps (L between 20 and 70 nm) to be obtained in a facile and controllable fashion. Finally, atomic layer

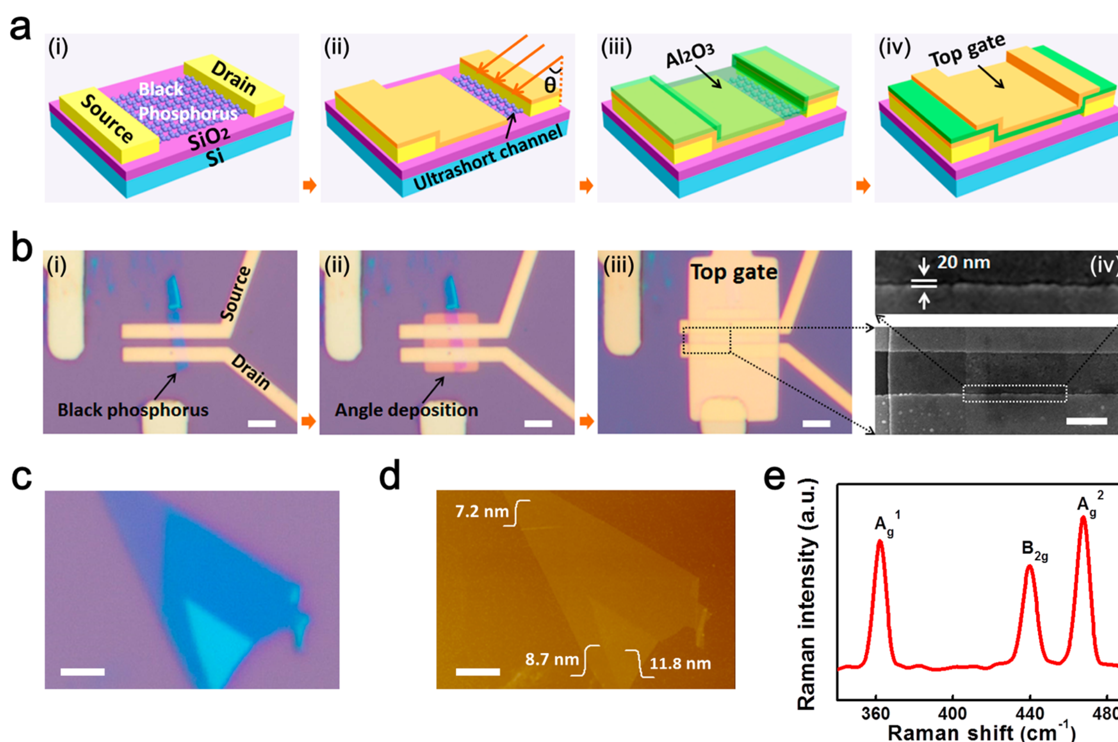

Figure 1. BP FET with a channel length of 20 nm fabricated by angle evaporation. (a) Schematic diagrams illustrating the fabrication process of the ultrashort channel length BP FETs. (i) "Long" channel BP FET obtained directly from EBL patterning and lift-off process; (ii) back-gated ultrashort channel BP FET obtained from angle evaporation; (iii) atomic layer deposition of 10 nm thick Al_2O_3 film as the gate dielectric; (iv) EBL patterning of the top gate for the ultrashort channel BP FET. (b) Optical microscope and SEM images of a representative ultrashort channel length BP FET at various stages of the fabrication process. Optical micrograph of a "long" channel (L = 1 μm) BP FET (i), a 20 nm back-gated BP FET obtained after the angle evaporation process (ii), and a 20 nm top-gated BP FET (iii). The scale bar for (i−iii) is 2 μm. Panel (iv) shows the SEM image of the same device with a 20 nm channel length. Scale bar: 1 μm. (c) Optical image of a representative BP nanoflake used in this study. Scale bar: 2.5 μm. (d) AFM image of the same BP nanoflake. Scale bar: 2.5 μm. (e) Raman spectra of the BP nanoflake used in this study.

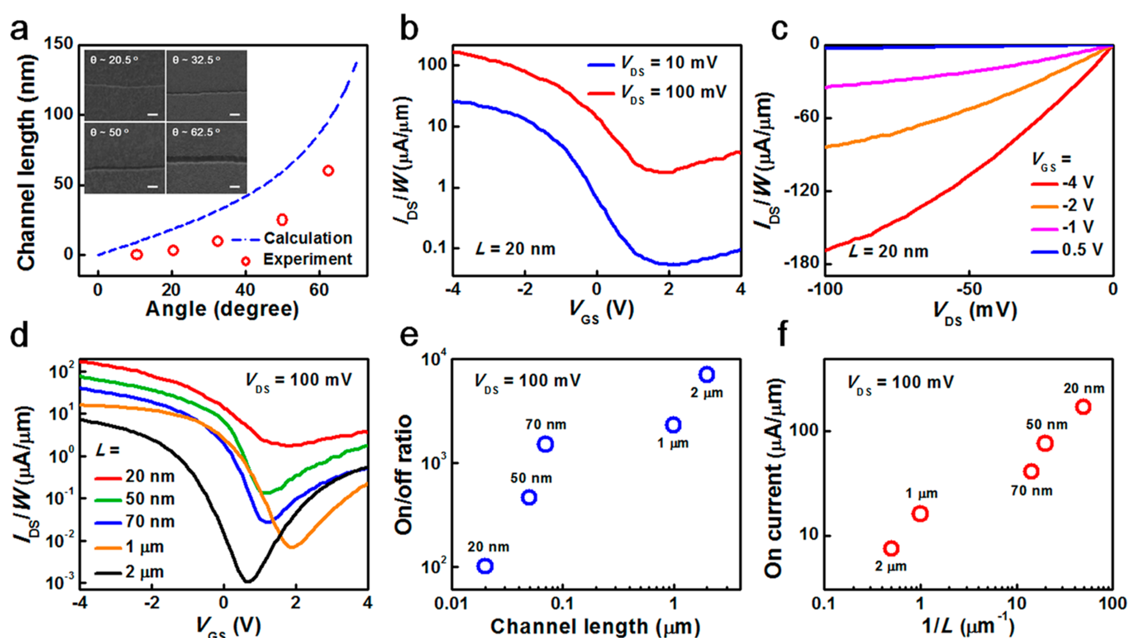

Figure 2. Electrical characteristics of ultrashort channel BP FETs. (a) Device channel length as a function of angle used during the metal deposition. Inset: SEM images of various channel lengths obtained. Scale bar: 50 nm. (b) Transfer characteristics ($I_{DS}-V_{GS}$) of a top-gated BP FET with a channel length of 20 nm. (c) Output characteristics ($I_{DS}-V_{DS}$) of the same device in (b). (d) Comparison of transfer curves for top-gated BP FETs with various channel lengths. (e) Device on/off current ratio plotted as a function of channel length. (f) Device on-current density plotted as a function of 1/L.

deposition (ALD) was used to deposit a 10 nm thick Al_2O_3 layer as the gate dielectric, followed by a third EBL patterning, metal evaporation, and lift-off process to obtain the top-gate electrode (Figure 1a(iii,iv)). Figure 1b shows the optical and scanning electron microscope (SEM) images of a representative top-gated 20 nm BP FET at various stages of the fabrication process. An ultrashort channel length of around 20 nm is evident from the SEM image in Figure 1b(iv). BP nanoflakes used in this study typically have thickness below 10 nm, and the representative optical micrograph and atomic force microscope (AFM) image are shown in Figure 1c,d, respectively. Figure 1e shows the Raman spectra obtained from the BP flake, in which three peaks can be observed at ~362, ~439, and ~467 cm^{-1}, corresponding to the A_g^1, B_{2g}, and A_g^2 phonon modes for pristine BP materials.[40]

The electrical characteristics of top-gated BP FETs with various channel lengths are presented in Figure 2. Figure 2a illustrates that the device channel length can be effectively controlled by varying the evaporation angle. The measured channel lengths from SEM (red open circle) agree well with the calculated values (blue dashed line) using the equation $L = t \times \tan(\theta)$, where L, t, and θ correspond to channel length, first electrode thickness (50 nm in this work), and evaporation angle, respectively. For ultrashort channel FETs, the gate oxide layer needs to be thin enough to allow effective electrostatic control of the channel carrier concentration by the gate electrode.[4] If the gate is not sufficiently strong, then the drain fights with the gate over the channel control, resulting in poor gate dependence. As shown in Supporting Information Figure S1, the transfer characteristics ($I_{DS}-V_{GS}$) of a back-gated BP FET with L = 20 nm measured at a drain-to-source voltage (V_{DS}) of 1 mV indicates that the back-gate bias cannot fully deplete the channel due to the 300 nm thick SiO_2 dielectric layer used. In this regard, the top gate with an ultrathin dielectric layer is needed for effective gate control. Figure 2b shows the transfer characteristics of a top-gated 20 nm long BP FET with a 10 nm Al_2O_3 gate dielectric measured at V_{DS} = 10 and 100 mV. The device exhibits a respectable on-current of 174 μA/μm and decent on/off ratio of 10^2 with V_{DS} = 100 mV. The current increases as the top-gate voltage sweeping from positive to negative, indicating the p-type transistor behavior. Output characteristics ($I_{DS}-V_{DS}$) of the same device with various top-gate biases (−4, −2, −1, and 0.5 V) are shown in Figure 2c. At small V_{DS} values, the drain current varies linearly with the drain voltage, indicating that the Schottky barrier is low and thin enough to allow Ohmic contact-like behavior between the Au metal and BP. More details about the Schottky barrier and contact resistance will be discussed later.

To assess the performance of the 20 nm top-gated BP FETs fabricated using our angle evaporation approach, the relevant figures-of-merit for recently reported BP-based FETs are summarized and compared in Table 1.[37,38,41,49,51,52] Due to the adoption of the smallest channel length (20 nm), our devices exhibit the highest on-state current (174 μA/μm) to date at a small source drain bias of 100 mV. Slightly higher on-current values of 200 or 350 μA/μm have been reported,[41,52] albeit at a much higher source drain bias of 2 V. To study

TABLE 1. Comparison of On-State Current for BP FETs Reported in the Literature

ref	contact material	channel length	V_{DS}	on-state current
this work	Au	20 nm	0.1 V	~174 μA/μm
49	Pd/Au	100 nm	0.5 V	~100 μA/μm
41	Ti/Pd/Au	300 nm	2 V	~350 μA/μm
52	Ti/Pd/Au	1 μm	2 V	~200 μA/μm
51	Ti/Au	1 μm	2 V	~100 μA/μm
37	Ti/Au	5 μm	0.1 V	~1 μA/μm
38	Ni	2 μm	0.2 V	~50 μA/μm

the channel length scaling of BP FETs, the transfer characteristics of five BP FETs with channel lengths of 0.02, 0.05, 0.07, 1, and 2 μm measured at V_{DS} = 100 mV are presented in Figure 2d. The device on/off current ratio (I_{on}/I_{off}) and unit-width-normalized on-current (I_{DS}/W) are extracted from Figure 2d and plotted as functions of channel length, as shown in Figure 2e,f, respectively. As the channel length aggressively scales from 2 μm to 20 nm, the average on/off current ratio decreases from $\sim 10^4$ to $\sim 10^2$, which can be attributed to the drain-induced barrier lowering (DIBL) and thermal-assisted tunneling process.[49] When the device channel length is extremely small, the drain bias will affect the energy barrier at the source side. As a result, the source barrier is now controlled simultaneously by both gate and drain voltages for ultrashort channel length devices, making such devices more difficult to turn off (Figure 2e). The extent of the short channel effects depends on the thickness of the semiconductor body relative to the channel length. The channel length of 20 nm is already approaching the thickness of the BP nanoflakes used in this work (around 10 nm). With such BP transistors exhibiting an on/off ratio of $\sim 10^2$ at an extremely small channel length of 20 nm, we consider the short channel effects to be relatively small and acceptable. In the future, the use of thinner or even monolayer BP nanoflakes could lead to ultrashort channel length transistors with even better immunity to short channel effects.

For the on-current, it is approximately inversely proportional to the channel length, as shown in Figure 2f, which agrees well with the classical FET theory. It is worth noting that compared with the "long channel" devices (L = 1 and 2 μm in Figure 2f), the on-current for "short channel" devices (L = 20, 50, and 70 nm in Figure 2f) is slightly below the predicted values from the linear extrapolation of the "long channel" data points. The reason is that the "long channel" devices were fabricated with a single-step EBL patterning with relatively thick (50 nm) Au S/D electrodes, while the "short channel" devices fabricated from angle evaporation had thinner (20 nm) S/D electrodes. The smaller S/D contact thickness leads to larger S/D series resistance, whose effect may not be significant for long channel devices but could be dominant when the

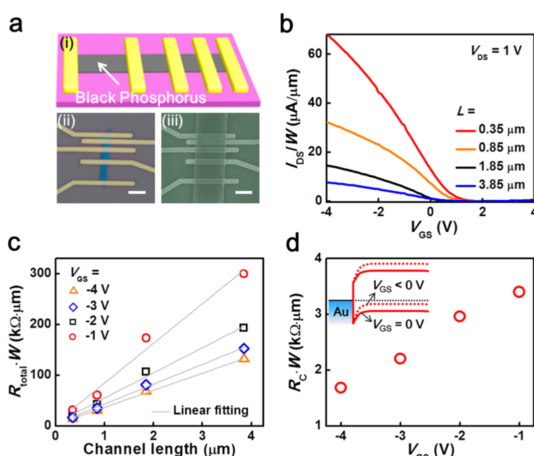

Figure 3. TLM method for extracting the contact resistance of BP FETs. (a) Schematic diagram (i), optical micrograph (ii), and SEM image (iii) showing the TLM structure with top-gated BP FETs of various channel lengths (0.35, 0.85, 1.85, and 3.85 μm) fabricated on the same BP nanoflake. A 10 nm thick Al_2O_3 layer is used as the top-gate dielectric in panel (iii). Scale bar: 4 μm. (b) Transfer characteristics of the top-gated BP FETs in the TLM structure measured at V_{DS} = 1 V. (c) Normalized total resistance (R_{total}) as a function of channel length for various gate biases. (d) Extracted contact resistance (R_c) as a function of the top-gate voltage. Inset: Energy band diagram of the Au/BP contact.

channel length becomes extremely small. Another possible mechanism that could lead to the slightly lower than predicted on-state current for ultrashort devices is the exposure of BP in ambient conditions, which is known to cause performance degradation in BP FETs.[51] We did our best to prevent the BP degradation during the fabrication from affecting the device performance by always passivating the sample with poly(methyl methacrylate) (PMMA) between the fabrication steps and storing the samples in an argon-filled glovebox when not in use. Nevertheless, the ultrashort channel devices did go through one more step of EBL patterning, metal deposition, and lift-off process before the Al_2O_3 capping compared with the long channel devices, which could contribute to momentary exposure in ambient conditions and thereby slightly degraded performance.

Contact resistance (R_c) plays an important role in transistor performance, particularly for those with ultrashort channel lengths.[7,49] Understanding the metal/BP contact is of great scientific and technological importance. The R_c can be extracted using the transfer length method (TLM) for BP FETs with long channel lengths.[49,53] In this case, the channel length is much larger than the carrier mean free path, and the channel can be considered to be entirely diffusive. A typical back- and top-gated BP FET array is presented in Figure 3a, showing four transistors fabricated on the same BP nanoflake used for TLM measurements. Figure 3b shows the transfer characteristics measured at V_{DS} = 1 V for devices with various channel lengths (0.35, 0.85, 1.85, and 3.85 μm). The maximum on-current occurs at a

top-gate voltage of −4 V. Figure 3c presents the normalized on-state total resistance (R_{total}), which includes both the channel resistance and R_c, plotted as a function of channel length. The decrease of R_{total} with more negative gate bias is simply due to the increase of carrier concentration in BP FETs. The S/D contact resistance ($2 \times R_c$) can be extracted from the *y*-axis intercepts of the linear fit (light gray line in Figure 3c). The extracted R_c (1688, 2208, 2964, and 3401 Ω·μm at a V_{GS} of −4, −3, −2, and −1 V, respectively) is then plotted as a function of top-gate voltage in Figure 3d. The R_c exhibits clear gate dependence and decreases monotonically as the top-gate voltage decreases from −1 to −4 V. This relationship can be explained using the energy band diagram of the metal/p-type BP junction presented as the inset of Figure 3d. A more negative gate bias (dashed line in Figure 3d inset) would result in a narrower Schottky barrier between the Au metal and p-type BP interface, which would facilitate the hole injection from the metal into the valence band of BP, resulting in smaller R_c.

For the long channel devices whose *L* is much larger than carrier mean-free path, the devices operate entirely in the diffusive regime and the contribution from the R_c is much smaller compared with the channel resistance. As a result, the R_c will have little effect on the extracted field-effect mobility. Nevertheless, for ultrashort channel devices, contribution from R_c becomes dominant and needs to be taken into consideration for precise evaluation of the intrinsic field-effect mobility. In order to do so, the extrinsic transconductance values (blue open circles in Figure 4a) are first extracted by differentiating the transfer curves (V_{DS} = 100 mV) presented in Figure 2b. The peak extrinsic transconductance of 50 μS/μm occurs at V_{GS} = −2 V. The intrinsic transconductance (g_{mi}) of the devices can be deduced by excluding the effect of R_c using the equation $g_{mi} = g_m/(1 - 2g_mR_c)$. Using the above equation, the peak intrinsic transconductance is found to be 70 μS/μm at V_{GS} = −2 V, as shown in Figure 4a (red open triangles). Both extrinsic (μ) and intrinsic (μ_i) field-effect mobilities can then be calculated using the equation $\mu = L(g_m/W)/(C_{ox}V_{DS})$, where C_{ox} is the unit-area capacitance of the 10 nm Al_2O_3 ($\varepsilon = 9.3$) gate dielectric. Using extrinsic (intrinsic) g_m values for the equation would lead to extrinsic (intrinsic) mobility accordingly. For our top-gated BP FETs with 20 nm channel length, the peak extrinsic and intrinsic field-effect mobilities were extracted to be ~12 and ~17 cm^2 V^{-1} s^{-1}, respectively, as shown in Figure 4b. It is worth noting that, although mobility values of greater than 100 cm^2 V^{-1} s^{-1} have been reported for BP FETs in some other reports cited in the table above, those devices are either long channel or back-gated devices. It is widely known that top-gating causes increased surface scattering due to the addition of the top-gate dielectric layer and short channel length

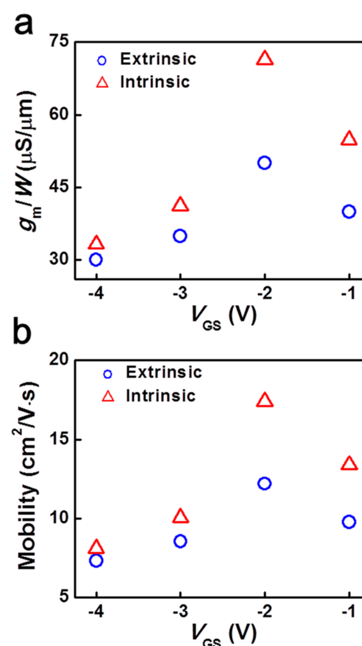

Figure 4. Extrinsic and intrinsic transconductance and field-effect mobility of the ultrashort channel length BP FET. (a) Device transconductance (normalized to the width of the BP nanoflake) at various gate biases measured at a V_{DS} of 100 mV. (b) Extrinsic and intrinsic field-effect mobility at various gate voltages.

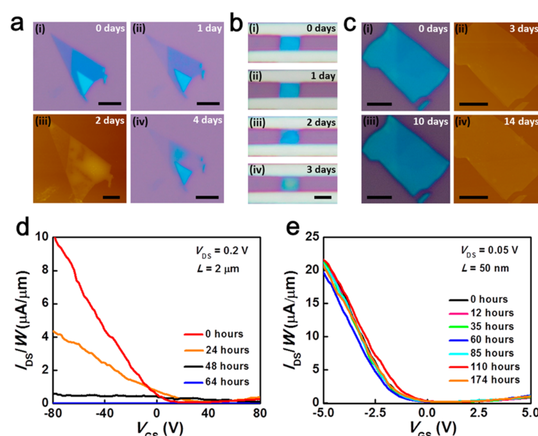

Figure 5. Air stability of back-gated and top-gated BP FETs. (a) Optical micrographs and AFM image of an unencapsulated BP nanoflake right after exfoliation (i) and after being stored in ambient conditions for 1 (ii), 2 (iii), and 4 (iv) days, showing obvious degradation. Scale bar for panels (i,ii,iv): 4 μm. Scale bar for panel (iii): 3 μm. (b) Optical micrographs of an unencapsulated back-gated BP FET right after fabrication (i) and after being stored in ambient conditions for 1 (ii), 2 (iii), and 3 (iv) days, showing similar degradation. Scale bar: 2 μm. (c) Optical micrographs and AFM images of a representative BP nanoflake passivated with 10 nm of Al_2O_3 right after exfoliation (i) and after being stored in ambient conditions for 3 (ii), 10 (iii), and 14 (iv) days. Scale bars: 2.5 μm. (d) Transfer characteristics of an unencapsulated back-gated BP FET measured after being exposed to ambient conditions for various amounts of time. (e) Transfer characteristics of an ultrashort (L = 50 nm) top-gated BP FET with a 10 nm thick Al_2O_3 gate dielectric measured after being exposed to ambient conditions for various amounts of time.

leads to carrier velocity saturation, both of which would result in reduced mobility. The mobility values of our top-gated ultrashort channel (L = 20 nm) BP FETs are comparable or slightly higher than those of the previously reported back-gated 100 nm channel length BP FETs whose intrinsic mobility is ~10 $cm^2 V^{-1} s^{-1}$.[49]

Pristine BP nanoflakes are known to be chemically unstable upon exposure to ambient conditions because the ambient adsorbates such as moisture irreversibly convert BP into PO_x compounds, fundamentally altering its electronic and material properties.[51] Figure 5a provides the optical micrographs and AFM image showing the degradation of an unencapsulated BP nanoflake on SiO_2/Si substrates when stored in ambient conditions. As time goes by, bubbles began to appear on the BP surface (AFM image) and the majority part of the BP flake disappeared after around 4 days. Similar behavior was observed in back-gated BP FETs, as shown in Figure 5b. Specifically, panels i–iv of Figure 5b correspond to the optical micrographs of an as-fabricated back-gated BP FET after being stored in ambient conditions for 0, 1, 2, and 3 days, respectively. Previous reports have shown that BP can be effectively protected from ambient degradation by appropriately chosen passivation layers.[51] Similar to previous reports, we have found that the Al_2O_3 gate dielectric deposited by ALD serves as an effective passivation layer. As an example, Figure 5c shows the optical micrographs and AFM images of a BP nanoflake passivated by 10 nm thick Al_2O_3 right after exfoliation. Compared with Figure 5a,b, no obvious degradation was observed on the encapsulated BP nanoflake after being stored for 14 days in ambient conditions. Figure 5d,e further compares the effect of Al_2O_3 passivating on the electrical characteristics of BP FETs. After fabrication and initial measurement (Figure 5d, red line), a back-gated BP FET (L = 2 μm) was exposed in ambient conditions. Within 64 h of exposure, the device on-current fell drastically from ~10 to ~0.2 nA/μm at a V_{DS} of 0.2 V, indicating severe degradation in BP. In contrast, for the top-gated ultrashort channel (L = 50 nm) BP FET, with the passivation from the 10 nm thick Al_2O_3 gate dielectric layer, no noticeable change was observed in the transfer characteristics even after the device was stored under identical ambient conditions for more than 1 week (174 h).

CONCLUSIONS

In summary, we report a facile method combining EBL and angle deposition to fabricate high-performance top-gated BP FETs with channel lengths down to 20 nm. With such small channel length, the devices exhibit one of the highest on-current (174 μA/μm for V_{DS} = 100 mV) to date for BP transistors. In addition, such ultrascaled BP transistors still preserve decent on/off current ratio (>10^2) and field-effect mobility (~17 $cm^2 V^{-1} s^{-1}$), which demonstrates the great potential of using BP for future high-performance ultimately scaled electronic and optoelectronic devices.

METHODS

Device Fabrication. The few-layer BP nanoflakes were mechanically exfoliated from bulk single crystals (Smart-element, Austria) and then transferred onto a heavily doped silicon substrate with a 300 nm thick SiO_2 dielectric layer. Prior to device fabrication, the substrate with BP nanoflakes was soaked in acetone for 1 h to remove the tape residues. Bilayer PMMA e-beam resists (MicroChem 495 A6 and 950 C2) were spin-coated (5000 rpm) onto the SiO_2/Si substrate followed by baking on a hot plate at 175 °C for 5 min. EBL (JEOL 840 with NPGS) was used to define the source/drain patterns, and 50 nm thick Au film was deposited using a thermal evaporator (Edward Auto 306) followed by lift-off process to form the S/D electrodes. The vacuum during evaporation was around 6×10^{-7} Torr. To achieve ultrashort channel length, a second EBL was carried out to open a window in the same bilayer PMMA resist across the channel region of the long channel BP transistors obtained in the previous step. The 20 nm thick Au film was subsequently evaporated intentionally at an angle (θ), allowing the existing 50 nm thick Au electrode to leave a shadow behind for the second metal deposition. This is done through the use of a tilting/rotating sample holder in the evaporator, allowing the metal evaporation angle to be precisely controlled from 0 to 90°. Additionally, it is necessary to ensure that the sample is always mounted at the same location on the sample holder in order to eliminate even the slightest possibility of variation in the deposition angle. This step forms ultrasmall gaps (L between 20 and 70 nm) between the S/D contacts. Atomic layer deposition (precursor: trimethylaluminum (TMA) and water; deposition temperature = 250 °C) was used to deposit a 10 nm thick Al_2O_3 layer as the gate dielectric. Finally, a third EBL patterning, gold evaporation, and lift-off were used to define the top-gate electrode.

Electrical Measurements. The electrical characteristics of the ultrashort channel length top-gated BP field-effect transistors were measured using a Signatone probe station and an Agilent B1500A semiconductor parameter analyzer. All measurements were conducted in ambient conditions.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b04036.

Transfer characteristics of back-gated BP FETs with a channel length of 20 nm (S1) (PDF)

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